Comparison Between the Most Popular Structures of Multilevel Inverters and the Packed U Cell Structure

Hakim KADRI*, Abdelhalim TLEMCANI**‡, Noureddine HENINI***

* Department of Electrical Engineering, Faculty of Technology, University of Médéa, Algeria, 26000

(kadri.hakim@univ-medea.dz, h_tlemcani@yahoo.fr, n.d.henini@gmail.com)

‡KADRI Hakim, 26000 Médéa, Algeria, Tel: +213776186040,

Fax: +213776186040, kadri.hakim@univ-medea.dz

Received: 09.07.2023 Accepted:09.08.2023

Abstract- the work compares three important topologies of multilevel inverters: diode-clamped inverters, flying capacitors, and cascaded H-bridge inverters. The comparison is based on parameters such as total harmonic distortion (THD) and electromagnetic interference (EMI) outputs. To carry out this comparison, simulations of these inverters are performed using MATLAB/Simulink. The simulations are conducted for three configurations: three-level single phase, three-level three phases, and five-level three-phase inverters. The simulation results obtained from MATLAB/Simulink serve as a basis for comparing the performance of these multilevel inverters. In addition to the comparative analysis of existing topologies, the work introduces a new structure called "packed u-cell 5" in MATLAB/Simulink. The performance of this new structure is evaluated by analyzing its THD characteristics. Furthermore, the work aims to improve the THD performance of the "packed u-cell 5" structure by implementing PID (Proportional-Integral-Derivative) control. The PID control technique is applied to reduce the THD generated by the inverter, enhancing its overall performance. Overall, the work involves a comprehensive study of various multilevel inverter topologies, comparing their THD and EMI outputs through simulations in MATLAB/Simulink. Additionally, it presents a novel structure, evaluates its THD performance, and explores the application of PID control to enhance its performance further.

Keywords: PID control, total harmonic distortion, electromagnetic interference, packed u cell inverter**.**

1. Introduction

To provide several output voltage levels with minimal harmonic content and supply more power to customers, the latest generation of equipment uses more active switches; these are power electronic converters. They are devices that can convert electrical energy from one form to another using power electronics principles [1]. They typically consist of semiconductor devices, such as diodes, transistors, thyristors, and passive components, such as capacitors and inductors. Power converters can manipulate voltage, current, and frequency to achieve the desired power conversion by switching these semiconductor devices on and off at high frequencies. In general, multilevel transformers offer significant advantages in improved power quality and reduced harmonics, making them suitable for low and medium-power applications. As research and development progresses, the potential for broader adoption of multilevel transformers in higher power applications continues to grow. In this regard, transforming grid interfaces and renewable energy are among the best applications for multilevel transformers. Neutral point converters (NPC), flying capacitor converters (FCC), and cascade h-bridge multilevel converters (CHB) are all examples of the types of multilevel transformers utilized in high-power industrial settings [2],[3]. However, as the number of voltage levels increases, these structures become more expensive and challenging to execute [4], offsetting some benefits, such as reduced harmonic distortion and high voltage transformation without a transformer, an enhanced variant of the traditional cascade H-bridge transformer, the packaged U-cell multilevel transformer (PUC), has been presented to solve these problems. The advantages of a PUC adapter can be achieved with fewer parts than in alternative topologies. No transformer is required to achieve high voltage conversion with low harmonic distortion [5]. In contrast, numerous studies have concentrated on a PUC converter in an assumed scenario where each switch in a multilayer inverter can function independently. Since the switches in a multilayer inverter must be powered together to produce the necessary voltage level at the output, this assumption must be changed. This means that the switching states of a set of switches must be considered during the design of multilevel switches. Some techniques have also been developed for controlling a PUC

inverter, such as the PUC5 inverter, which provides voltage balance to capacitors without resorting to a feedback loop. This is significant because multilayer transformers only function correctly with balanced capacitor voltages. Research is performed to establish precise models and control strategies for efficient and dependable operation of the PUC multilevel converter, which provides a more cost-effective and streamlined solution than alternative topologies. PUC5 inverter's proposed methods aim to achieve a balanced capacitor voltage without a feedback loop. There are two potential answers to this, each with its benefits and drawbacks, H. Vahedi and coworkers put forth the first potential answer. As of 2016, it employs phase-order pulse-width modulation (PD-PWM). This technique employs a switch state table and four shift plane vectors. The inverter's switching states can be carefully managed to achieve voltage balance across the capacitors. However, the voltage across the capacitor must be stable for this strategy to work. One significant drawback of this method is the capacitor size that must be used. In 1981, A.M. Abarzadeh and coworkers introduced a new approach to address the problems with the original method. Two plane-shifted triangular carriers and six logic gates are all that are required for this procedure. Capacitor voltages can be equalized by carefully manipulating the triangle mounts and applying logic gates. When compared to the conventional method, this innovation allows for a smaller capacitor size to be used. However, remember that this method adds considerably more work and complexity to your computations. Practical implementations may encounter difficulties as complexity and processing overhead rise. In conclusion, the first method based on PD-PWM necessitates a giant capacitor. Still, it offers a more uncomplicated application, while the second option, based on triangular vectors and logic gates, permits a smaller capacitor but imposes more stringent computing requirements. The best approach for a given task depends on those needs and constraints [6]. We can obtain a considerable amount of THD by simulating this proposed inverter.

2. Diode-Clamped Multilevel Inverter

Diode-clamped inverters, also known as neutral-point-clamped inverters, are often used to change DC power into AC power. These inverters see extensive use in a wide range of settings, from high-voltage power transmission to motor drives and renewable energy systems [7].

The basic principle of a diode-clamped inverter is to generate a stepped waveform by combining several voltage levels. This is achieved by connecting a series of capacitors and diodes in parallel with the inverter switches [8]. The block diagram of the neutral point clamped 3 levels is depicted in Figure 1.

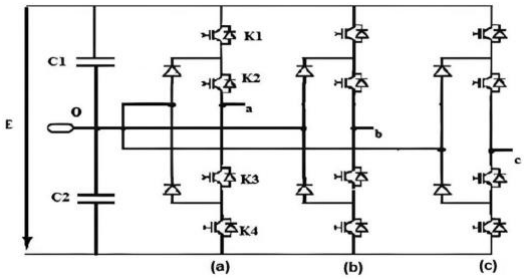


Fig. 1. NPC inverter three levels

The block diagram of the NPC 3 levels three phases is depicted in Figure 2.

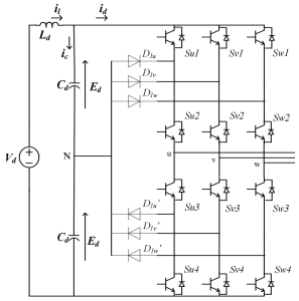


Fig. 2. NPC three-level three phase

Each phase of the converter's output voltage and switching pattern. are shown in Table 1.

Table 1. Switching pattern and output voltage generated for the converter

	Switch Code				Output Voltage
	S_{u1}	S_{u2}	S_{u3}	S_{u4}	v_{uN}
Switching State	On	On	Off	Off	E_d
	Off	On	On	Off	0
	Off	Off	On	On	$-E_d$

Diode-clamped inverters, a type of multilevel topology in which a diode is employed to clamp the dc bus voltage to achieve steps in the output voltage, are popular. In this configuration, the semiconductor power components can only withstand a reverse voltage of 50% of the DC source voltage. The ideas employed in the 3-level topology can be extrapolated to topologies with any number of levels [9].

The block diagram of the neutral point clamped five levels in three phases is depicted in Figure 3.

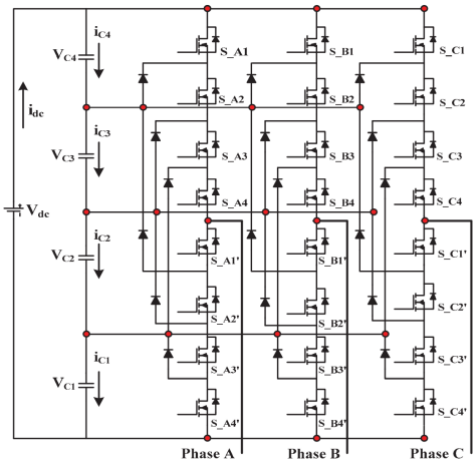


Fig. 3. A Five-Level three-phase NPC structure [10].

Switching states for 5-level DCC is shown in Table 2.

Table 2. Switching states for 5-level DCC [10].

Switching State $S\_A1\ S\_A2\ S\_A3\ S\_A4$ $S\_A1'\ S\_A2'\ S\_A3'\ S\_A4'$	Voltage Level	Line Voltage
11110000	4	V_{dc}
01111000	3	$3V_{dc}/4$
00111100	2	$V_{dc}/2$
00011110	1	$V_{dc}/4$
00001111	0	0

The neutral point n is the reference point for the output phase voltage to synthesize a five-level voltage across phases and employ staircase voltage synthesis. The staircase voltage synthesis method commonly uses a bank of power electronic switches to create the necessary voltage levels. Five distinct voltage levels must be produced here. First, we have V1, then V2, then V3, then V4, then V5, etc. We can utilize five switch configurations to generate these values between phases.

As an illustration of the utility of these switch configurations, consider the following:

1) Switch Combination 1: Consequently, the voltage at the output

$$V_{an} = V_{dc}/4 \quad (1)$$

Turn on all upper switches $S_1\_S_4$.

2) Switch Combination 2: Consequently, the voltage at the output

$$V_{an} = V_{dc}/2 \quad (2)$$

Turn on three upper switches $S_2\_S_4$ and one lower switch S_1'.

3) Switch Combination 3: Consequently, the voltage at the output

$$V_{an} = 0 \quad (3)$$

Activate the top two switches $S_3\_S_4$ and two lower switches S_1' and S_2'.

4) Switch Combination 4: Consequently, the voltage at the output

$$V_{an} = -V_{dc}/4 \quad (4)$$

Turn on one upper switch and three lower switches $S_1'\_S_3'$.

5) Switch Combination 5: Consequently, the voltage at the output

$$V_{an} = -V_{dc}/2 \quad (5)$$

Turn on all lower switches $S_1'\_S_4'$.

3. Flying Capacitor Multilevel Inverter

Maynard and Foch invented a new kind of multilevel inverter in 1992 called a flying capacitor multilevel inverter, which uses capacitors instead of clamping diodes. Comparable to a diode-clamped inverter but uses capacitors instead of diodes. The flying capacitor multilayer inverter is a circuit topology with many switch and capacitor stages. In a typical configuration, a capacitor is placed in the middle of a sequence of switches at each level. Power electronic devices such as insulated-gate bipolar transistors (IGBTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) are frequently used as switches. The output of the inverter can provide numerous voltage levels thanks to the flying capacitors. The inverter can generate stepped voltage waveforms at the AC output by selectively connecting the capacitors to different voltage levels on the DC side (also called the input side). The voltage across each capacitor in the ladder is varied to alter the output voltage. A sine wave or a multilayer waveform can be generated by modulating the voltage between an inverter's output terminals correctly. The circuit topology of a flying capacitor multilevel inverter single-phase three-level and five-level, three phases three-level and three-phase five-level are depicted respectively in Fig. 4-5-6. The capacitors on the dc side are connected in a ladder configuration with different voltages across each rung. [7].

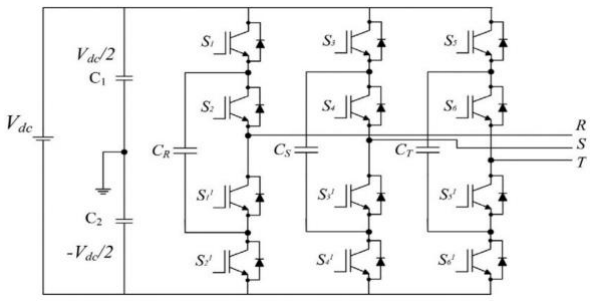


Fig. 4. Three-phase three-level flying capacitor converter

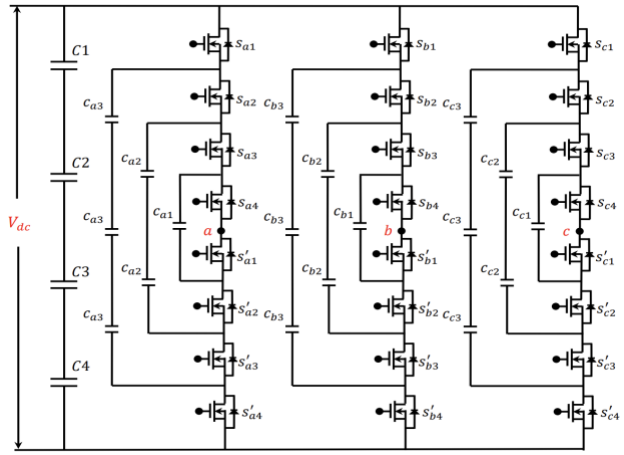


Fig. 5. Flying capacitor five level three phase

In addition to being suitable for HVDC (strong Voltage Direct Current) applications, the flying capacitor multilevel converter's many benefits include its versatile switch mode operation, strong protection capabilities for power devices, and easy control of absolute power and reactive power. Capacitor charging and discharging must be balanced, which poses a problem for these converters and necessitates a variety of intermediate-level switch configurations. The voltage synthesis of a five-level capacitor-clamped converter is more versatile than that of a diode-clamped converter. The five-level capacitor-clamped converter provides greater control and flexibility in power conversion applications, allowing for a more extensive range of output voltage levels.

The voltage of the five-level phase-leg output concerning the neutral point n is shown in Fig.6(b), V_{an}, can be generated by the following set of toggles.

1) Switch Combination 1: As a result, the output voltage

$V_{an} = V_{dc}/2$ (6)

turn on all upper switches S_1_S_4.

2) Switch Combination 1: As a result, the output voltage

$V_{an} = V_{dc}/4$ (7)

there are three combinations:

a) S_1, S_2, S_3, S_1' (V_{an} = $V_{dc}/2$ of upper $C_4's$-$V_{dc}/4$ of C_1);

b) S_3, S_4, S_3', S_4' (V_{an} = $V_{dc}/2$ of C_2 -$V_{dc}/2$ of lower C_4);

c) S_1, S_3, S_1', S_3' (V_{an} = $V_{dc}/2$ of upper $C_4's$ -$3V_{dc}/4$ of $C_3's$ +$V_{dc}/2$ of $C_2's$ -$V_{dc}/4$ of C_1);

d) S_1, S_4, S_2', S_3' (V_{an} = $V_{dc}/2$ of upper $C_4's$ -$3V_{dc}/4$ of $C_3's$ +$V_{dc}/4$ of C_1);

e) S_2, S_4, S_2', S_4' (V_{an} = $3V_{dc}/4$ of $C_3's$ − $V_{dc}/2$ of $C_2's$ +$V_{dc}/4$ of C_1-$V_{dc}/2$ of lower $C_4's$);

f) S_2, S_3, S_1', S_4' (V_{an} = $3V_{dc}/4$ of $C_3's$ − $V_{dc}/4$ of C_1-$V_{dc}/2$ of lower $C_4's$).

4) Switch Combination 1: As a result, the output voltage

$V_{an} = -V_{dc}/4$

(8) There are three combinations:

a) S_1, S_1', S_2', S_3' (V_{an} = $V_{dc}/2$ of upper $C_4's$-$3V_{dc}/4$ of $C_3's$);

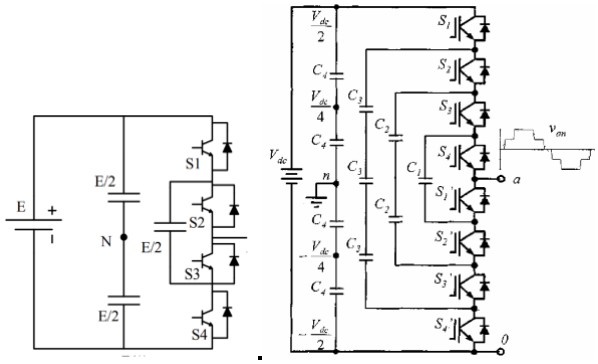
b) S_4, S_2', S_3', S_4' (V_{an} = $V_{dc}/4$ of C_1-$V_{dc}/2$ of lower $C_4's$);

c) S_3, S_1', S_3', S_4' (V_{an} = $V_{dc}/2$ of $C_2's$-$V_{dc}/4$ of C_1-$V_{dc}/2$ of lower $C_4's$);

5) Switch Combination 1: As a result, the output voltage

V_{an}=- $V_{dc}/2$

(9) turn on all lower switches S_1'_S_4' [11].



(a) (b)

Fig. 6. Three Level single-phase Structures of a Flying Capacitor Inverter. (a) three level. (b) five level.

Switching states for the 5-level flying capacitor inverter are shown in Table 3.

Table 3. The multilevel inverter switching sequence [12].

S.No	S1	S2	S3	S4	S5	S6	S7	S8	Output Voltage
1	1	1	1	1	0	0	0	0	4E
2	0	1	1	1	0	0	0	1	3E
3	0	0	1	1	0	0	1	1	2E
4	0	0	0	1	0	1	1	1	E
5	1	1	1	0	1	0	0	0	-E
6	1	1	0	0	1	1	0	0	-2E
7	1	1	1	0	1	1	1	1	-3E
8	0	0	0	0	1	1	1	1	-4E

4. H-Bridge Inverter

The one-phase design of an m-level cascaded inverter is shown in Fig. 7. This setup contains several tiers of inverters, each of which is an H-bridge inverter connected to its separate source of direct current (SDCS). Each inverter stage employs a set of switches labeled S1, S2, S3, and S4 to regulate the output voltage. Each inverter stage in this arrangement can produce +Vdc, 0 Vdc, and -Vdc at its output. The output voltage can be adjusted by manipulating the on/off states of the four switches. The possible permutations of switch states determine the polarity and magnitude of the output voltage.

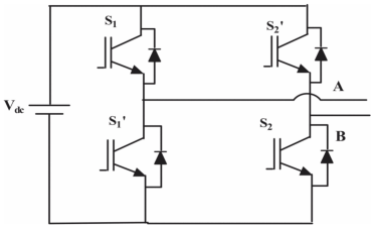


Fig. 7. Three-level H-bridge cascade inverter arm [13].

The voltage outputs for each possible switch configuration are listed below.

S1 and S3 are active, whereas S2 and S4 are disabled: The DC voltage output from this setup is +Vdc, which is positive.

When S2 and S4 are activated, S1 and S3 are deactivated. The DC voltage produced by this setup is negative, at -Vdc.

There is no power to any of the devices (S1, S2, S3, or S4): In this setup, there will be no output voltage (0 Vdc).

The cascaded m-level inverter can generate different output voltage levels by selecting and activating the switches in each inverter stage. The possible range of voltage steps is proportional to the number of levels, m [4].

The output voltage of a CHB MLI with K sources will have H discrete levels. The relations are

H=2K+1 (10)

Number of source/number of bridges (K)=(H-1)/2 (11)

Number of switches(n)=(m×2)-2 (12)

Max voltage=K×Vdc (13)

H=number of output voltage level

K= number of bridges.

N= number of switching devices.

The block diagram of the cascaded h bridge five levels is depicted in Figure 8.

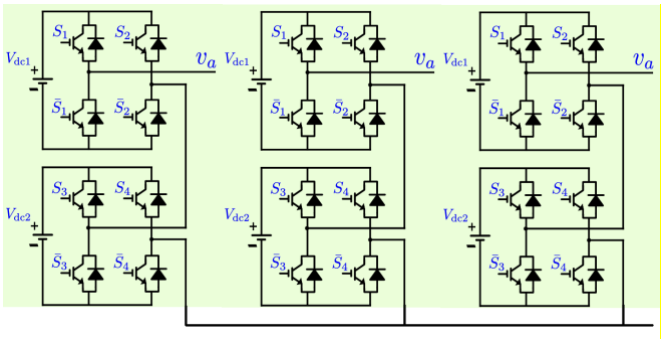


Fig. 8. Five levels cascade H-bridge inverter [13].

Switching states for the 5-level cascaded h bridge inverter are shown in Table 4.

Table 4. Switching state for the 5-level conventional configuration [14].

Modes	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$2V_{dc}$	on	off	off	on	on	off	off	on
V_{dc}	on	off	off	on	off	off	on	on
0	off	off	off	off	off	off	off	off
$-V_{dc}$	off	on	on	off	off	off	on	on
$-2V_{dc}$	off	on	on	off	off	on	on	off

5. PUC inverters

5.1. Five-level PUC inverter topology

The block diagram of the packed u-cell five-level inverter is depicted in Figure 9.

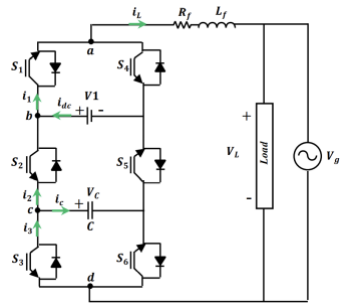


Fig. 9. Schematic diagram of Pucked U Cell Inverter [6].

Switching states for the PUC inverter are shown in Table 5.

Table 5. PUC inverter state-switching

State	V_{ab}	s_1	s_2	s_3
1	V_{dc}	1	0	0
2	V_{dc}-V_{C1}	1	0	1
3	V_{C1}	1	1	0
4	*0*	1	1	1
5	*0*	0	0	0
6	-V_{C1}	0	0	1
7	V_{C1}-V_{dc}-	0	1	0
8	-V_{dc}	0	1	1

Compared to other multi-level inverters, the five-level PUC (Packed U-Cell) inverter has fewer components and produces AC power with lower total harmonic distortion (THD). It is frequently used in different systems, including renewable energy generators, motor drives, and uninterruptible power generators. A five-level PUC inverter's primary circuit diagram includes a DC power source, six electronic switches, and a capacitor. In most cases, pulse width modulation (PWM) techniques are used to operate switches made out of insulated gate bipolar transistors (IGBTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs). The five-level PUC inverter works by combining the voltages of the capacitors to produce a waveform with varying voltages. The maximum output voltage is directly proportional to the capacitor voltage. While the circuitry is identical between the PUC7 and PUC5 variations, the capacitor voltage is fixed at different levels. The output waveform of a five-level PUC inverter can display five different voltage levels because of the capacitors' strategic placement. These voltage settings enhance the inverter's functionality by decreasing THD. The five-level inverter sacrifices output voltage levels but has advantages in size, complexity, and cost compared to higher-level topologies. The five-level PUC inverter decreases system complexity and expense by using fewer components. It also aids in keeping the inverter's price and footprint to a minimum. The inverter's efficiency and dependability have been improved due to the reduced number of components required for its operation [15].

In conclusion, the five-level PUC inverter is a circuit architecture that uses capacitors to produce a waveform with several voltage levels. It is well-suited for use in a wide range of power electronic applications due to its combination of low THD, decreased component count, and cost-effective design [16].

During each half-cycle of the sine wave source, the electronic power switches in a five-level PUC inverter will alternate between being on and off. The inverter may produce the desired output voltage waveform by adjusting the switching states.

The block diagram Conducting paths for switching states is depicted in Figure 10.

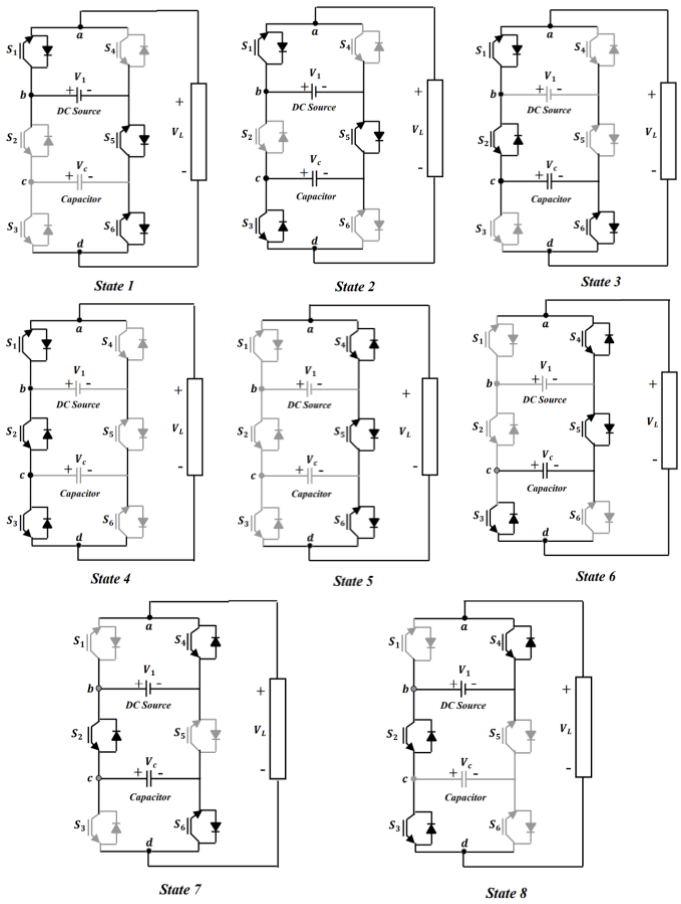


Fig. 10. Conducting paths for switching states [6].

The five-level PUC inverter has just six switch states since two switch states are skipped for every cycle. The following examples have been removed:

Switch state 3 (positive cycle discharge): The capacitor is not discharged by the inverter during the positive half cycle of the sine wave source. To preserve the charge on the capacitors, the electronic power switches related to the discharge are disabled.

During the negative half cycle of the sine wave source, the inverter will not charge the capacitor and enter Switching State 7. Capacitors retain their charge because the electrical power switches are disabled [5].

In the same vein as the PUC7 variation, the remaining switch states will be:

Switch state 1: positive charge cycle

Switch state 2: positive discharge cycle

Switch state 4: negative charge cycle

Switch state 5: negative discharge cycle

Switch state 6: Zero voltage state (neutral)

The five-level PUC inverter delivers the necessary voltage levels while reducing complexity and the number of switching operations by skipping these two switching states per cycle. Inverter performance is preserved while the control technique is simplified, and switching losses are minimized with this method [15].

The PUC5 configuration during charging and discharging is depicted in Figure 11.

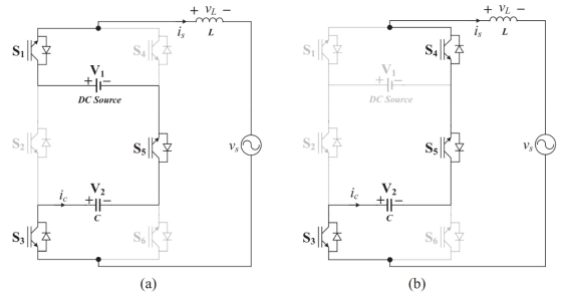


Fig. 11. PUC5 configuration during (a) charging and (b) discharging [17].

The packed u cell Connection and voltage of capacitors are shown in Table 6.

Table 6. Connection and voltage of capacitors [5].

Possible states	Connected to DC supply	Connected to load	Capacitor voltage
1	NO	NO	No effect
2	YES	YES	Charging
3	NO	YES	Discharging
4	NO	NO	No effect
5	NO	NO	No effect
6	NO	YES	Discharging
7	YES	YES	Charging
8	YES	NO	No effect

5.2. Design and Operation of a PUC Inverter

Six semiconductor switches and two DC links are in a single-phase PUC (Packed U-Cell) inverter setup. The switches are wired in three sets of two that operate in opposition. A U-Cell is formed when a DC link links together four switches. The complete PUC inverter consists of these U-Cells. A DC supply is used for one of the DC links on the upper side, while a DC capacitor is used for the DC link on the lower side. A switching method regulates the DC capacitor voltage. The voltage across the capacitor can be controlled by correctly toggling the semiconductor. The voltage of the DC capacitor can be accurately controlled by using switches efficiently controlled using this technique. The upper two switches have twice the capacity of the lower four. The switches' exposure to voltage stress is to blame for this rating discrepancy. The upper set of switches needs to be able to handle the higher DC supply voltage. In contrast, only half of the DC supply voltage is applied to the bottom pairs of switches due to the capacitor voltage they are connected to. The PUC inverter is set up to accept DC input and output an AC waveform with a high frequency. The switches' ability to operate in parallel assures the production of an AC output, which has several potential uses. The inverter's control scheme and modulation techniques are crucial to producing the correct output voltage and current characteristics and keeping the switches and system running smoothly and reliably [18].

The proposed open-loop switching algorithm for sensorless PUC5 inverter self-voltage balancing is depicted in Figure 12.

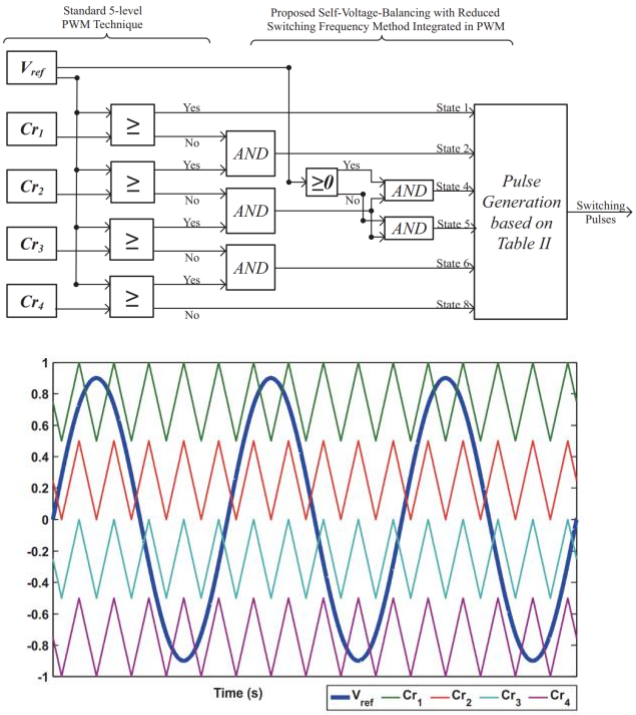


Fig. 12. Proposed open-loop switching algorithm for sensorless PUC5 inverter self-voltage balancing [17].

6. Simulation Results

Simulation of multilevel inverters is used to verify PWM's performance, and the simulation is done under Matlab/Simulink.

Table 7. Simulation parameters for CHB, NPC, and FC inverters

parameters	value
DC-link-voltage	100 V
Resistance	10 Ω
Flying Capacitor	1/3e-6 F

Table 8. Simulation parameters for PUC5 inverter

parameters	value
DC-link-voltage	100 V
Resistance	100 Ω
capacitor	3500e-6 F
inductance	250e-3 H
Kp	0.214441047073489
Ki	0.157791984137529
Kd	0.0705872353484475

The SPWM of NPC three-level and five-level topology is depicted in Figure 13 and Figure 18. figure 15 and 17, and 20 show us That THD decreases with increasing levels and number of phases.

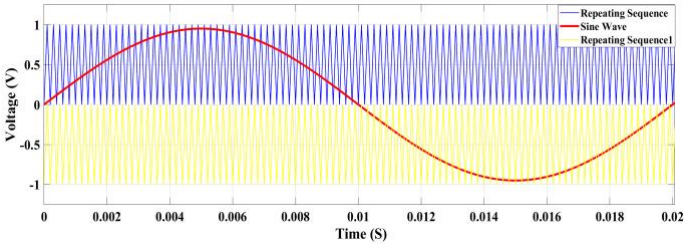


Fig. 13. SPWM of the NPC three-level topology

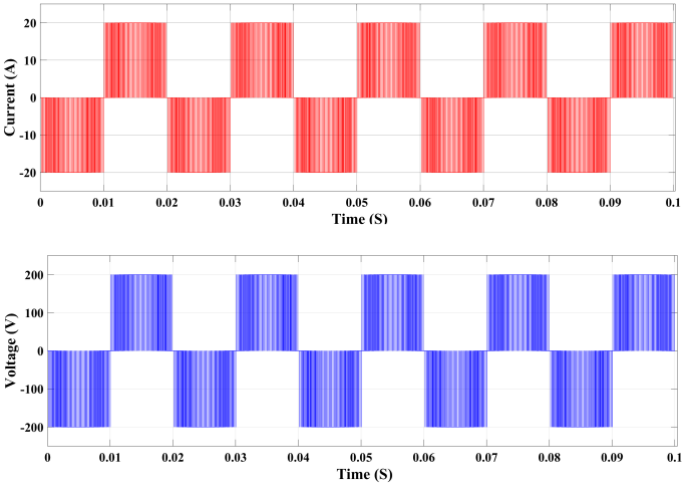


Fig. 14. Output voltage + current of the NPC three-level topology

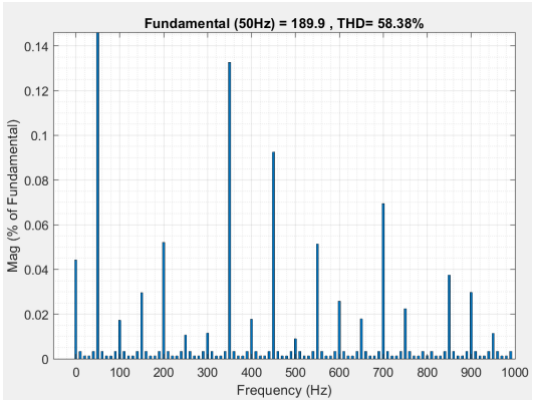


Fig. 15. THD of NPC three-level single phase

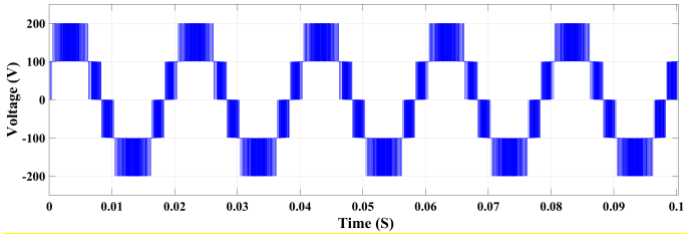


Fig. 16. Line voltage of NPC three level three phase

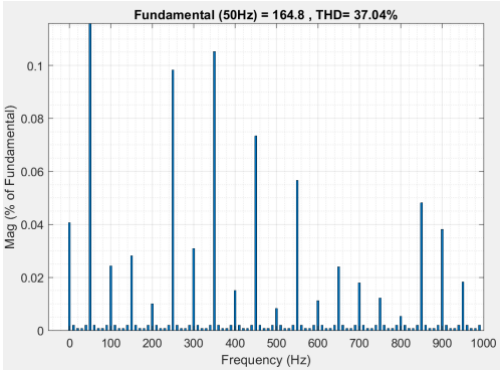


Fig. 17. THD of NPC three level three phase

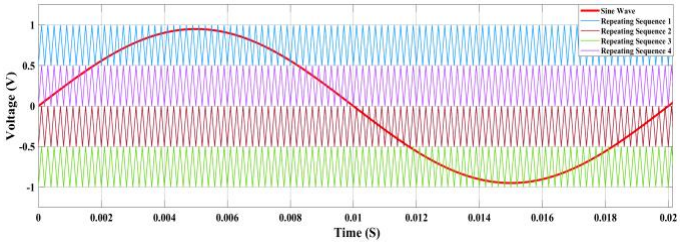


Fig. 18. SPWM of the NPC five-level topology

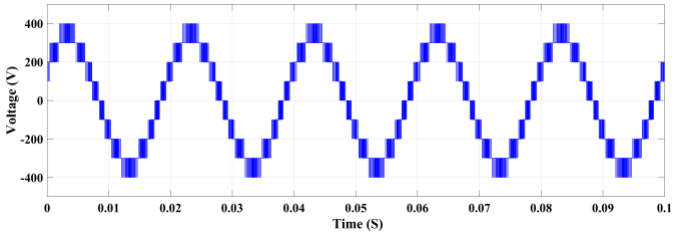


Fig. 19. Line voltage of NPC five level three phase

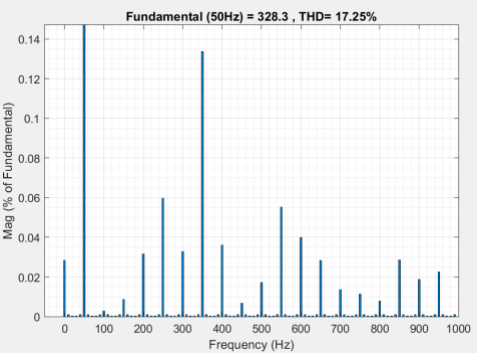


Fig. 20. THD of NPC five level three phase

The SPWM of the FC three-level and five-level topology is depicted in Figure 21 and Figure 26. figure 23 and 25, and 28 show us The THD decreases with increasing levels and the number of phases

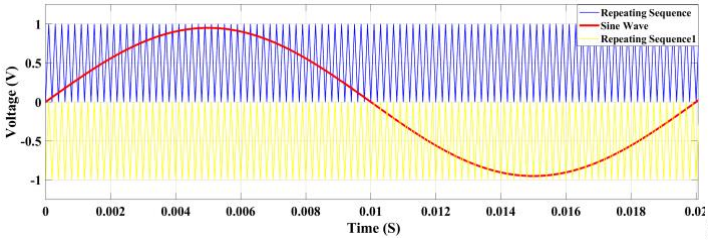


Fig. 21. SPWM of the FC three-level topology

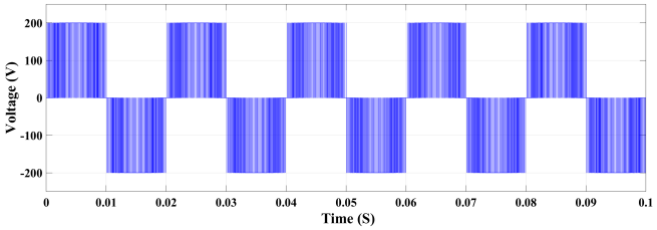


Fig. 22. Output voltage of FC three-level single phase

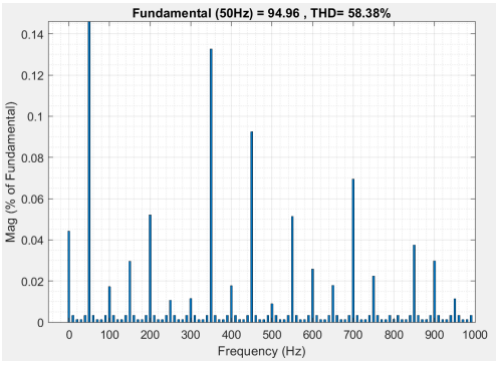


Fig. 23. THD of FC three-level single phase

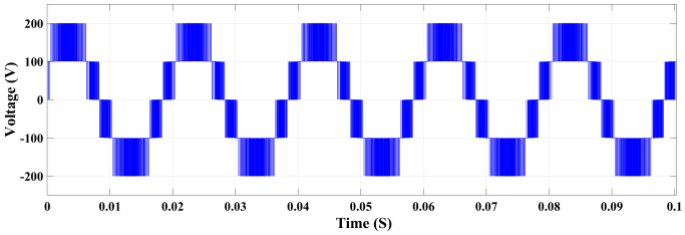


Fig. 24. Line voltage of FC three level three phase

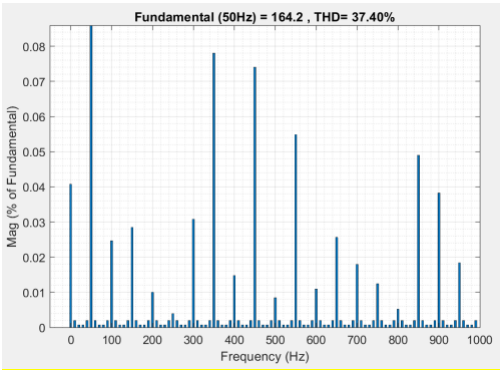


Fig. 25. THD of FC three level three phase

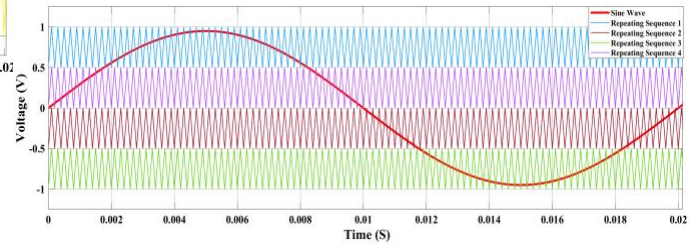


Fig. 26. SPWM of the FC five-level topology

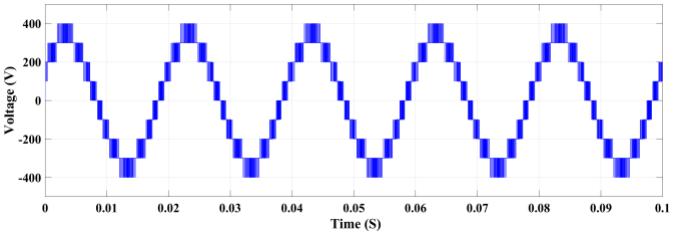


Fig. 27. Line voltage of FC five level three phase

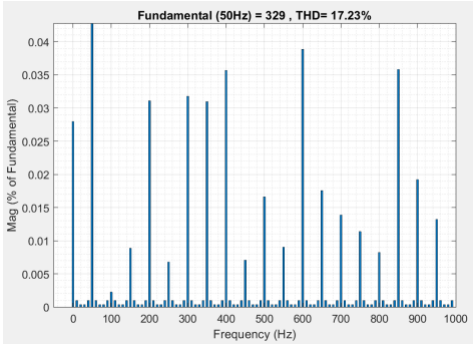


Fig. 28. THD of FC three level three phase inverter

The SPWM of the CHB three-level and five-level topology is depicted in Figure 29 and Figure 34. figure 31 and 33, and 36 show us The THD decreases with increasing levels and the number of phases

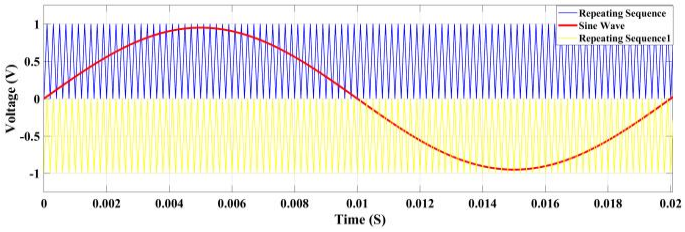


Fig. 29. SPWM of CHB three-level topology

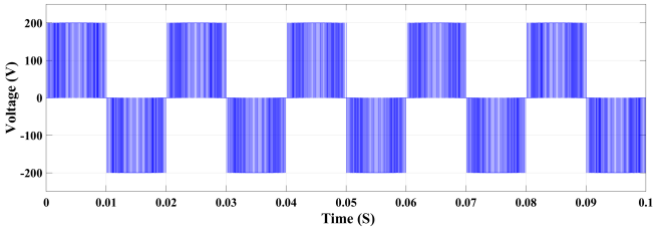


Fig. 30. Output voltage of CHD three level single phase topology

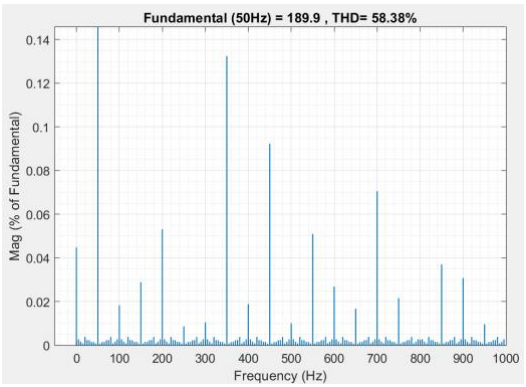


Fig. 31. THD of CHB three-level single phase

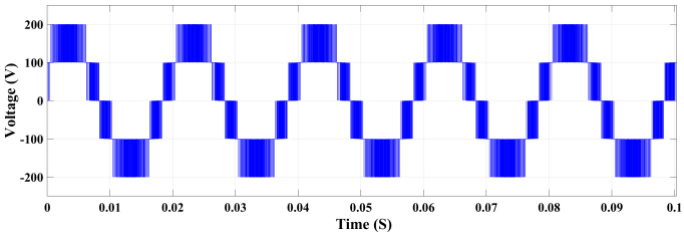


Fig. 32. Line voltage of CHB three level three phase

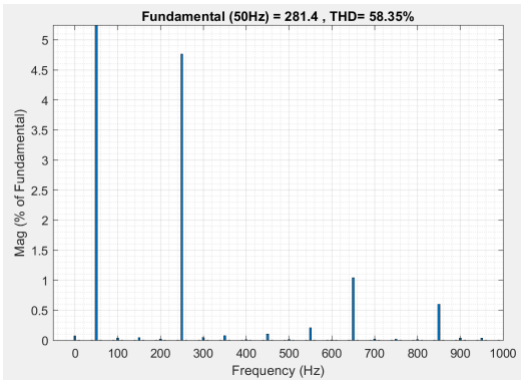


Fig. 33. THD of three-level three-phase CHB

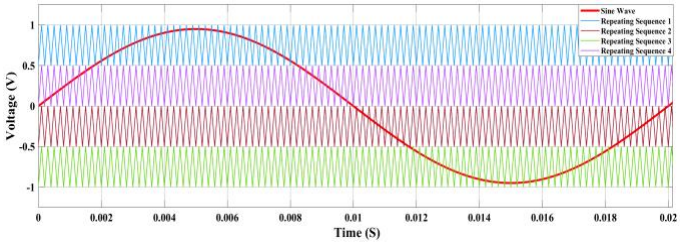


Fig. 34. SPWM of the cascaded H-bridge five-level topology

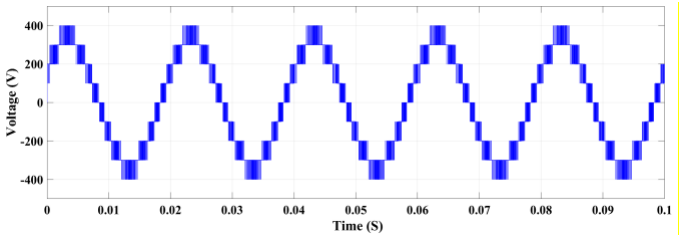


Fig. 35. CHB five-level three-phase line voltage

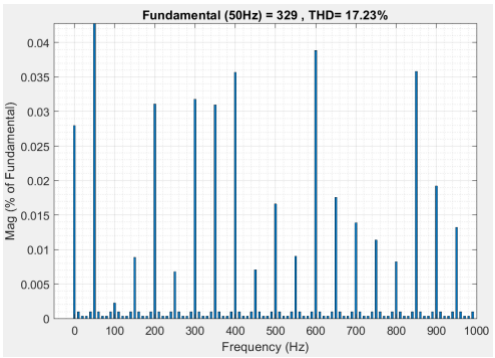


Fig. 36. THD of five level three-phase CHB

The output voltage and output current of the packed u- cell five topology is depicted in Figure 37. Figure 40 shows that The THD decreases from 17,52 in Figure 39 to 1,73 when we add a PID.

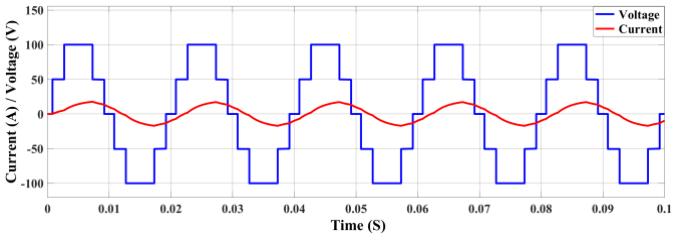


Fig. 37. Output voltage + current of the PUC5 topology

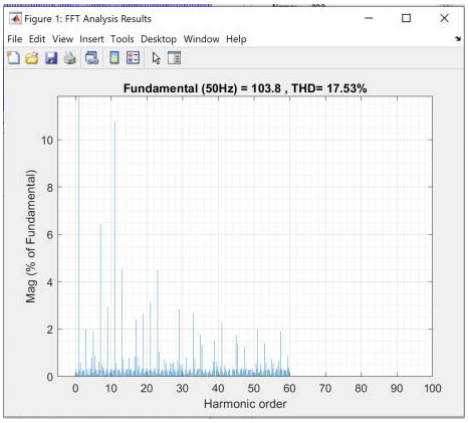


Fig. 38. Output Voltage FFT Analysis of PUC5 inverter

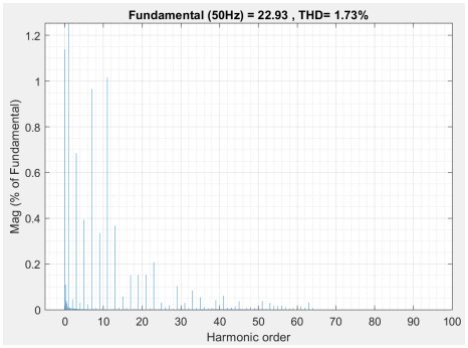


Fig. 39. Output Voltage FFT Analysis of PUC5 inverter with PID.

The THD voltage between the most popular inverters is shown in Table 3.

Table 9. The THD voltage between the most popular inverters

Modes (Voltage)	THD in ٪
NPC, FC, and CHB inverters 3 level 1 phase	**58,38**
NPC, FC, and CHB inverters 3 level 3 phase	**37,40**
NPC, FC, and CHB Inverters 5 level 3 phase	**17,23**
PUC 5 inverter	**17,53**
PUC 5 with PID controller	**1,73**

Figure 40 and 41 and 42, and 43 show us The THD of the multilevel inverters.

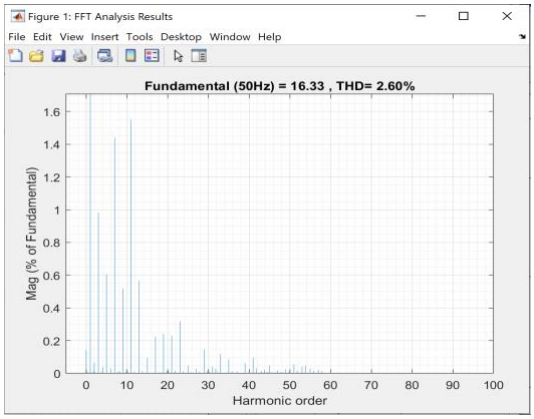


Fig. 40. Output current FFT Analysis of PUC5 inverter

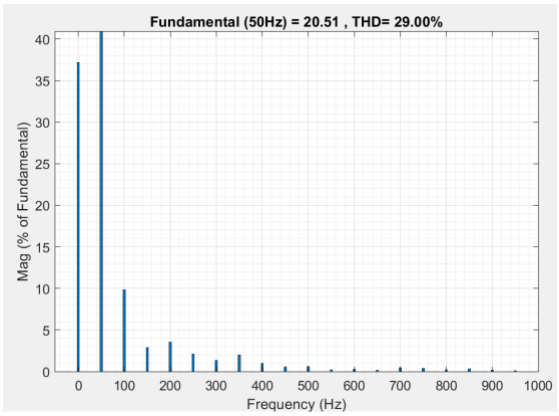


Fig. 41. Output current FFT Analysis of CHB 5 level 3 phase inverter

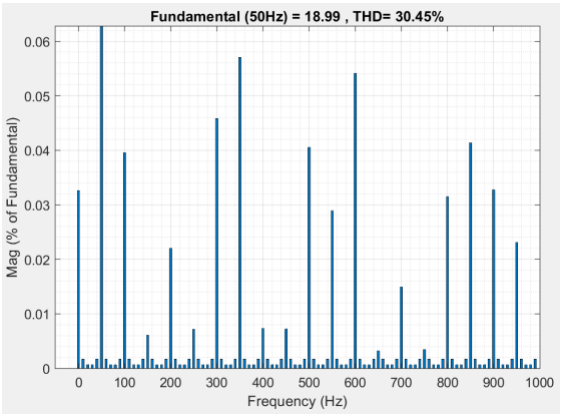


Fig. 42. Output current FFT Analysis of FC 5 level 3 phase inverter

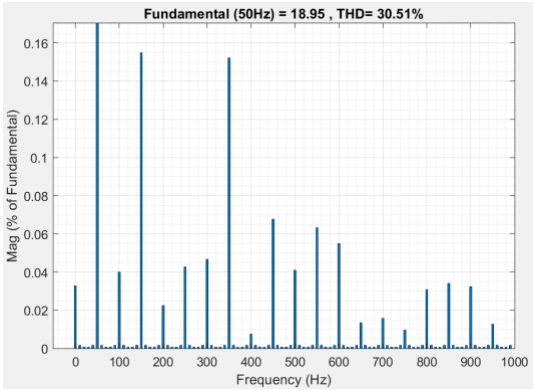


Fig. 43. Output current FFT Analysis of NPC 5 level 3 phase inverter

The packed U-cell inverter is shown in the following table. Compared to NPC, FC, and CHB transformers, although it has the fewest components, it produces the lowest current THD.

Table 10. the total harmonic distortion current between the most popular inverters

Modes (Current)	THD in ٪
NPC inverter 5 level 3 phase	**30,51**
FC Inverter 5 level 3 phase	**30,45**
CHB Inverter 5 level 3 phase	**29,00**
PUC 5 inverter	**2,60**

7. Conclusion

This paper presented the most popular inverters: neutral point clamped flying capacitor and cascaded h-bridge. Comparison between these topologies showed us a decrease of the total harmonic distortion between the single phase, the three phases three-level, then the five-level three-phase, but these topologies required more number of diodes and capacitors after we used another topology called packed U Cell 5, required fewer diodes and capacitors and giving us The value of a Total Harmonic Distortion voltage is 1.73% and a current of 2.60%.

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